ATP Industrial Grade CFast Card Specification

Version 2.3

ATP Electronics, Inc.

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Revision History

Date	Version	Revision History
April 7th, 2014	2.0	- New BOM Release
Jan. 28th, 2015	2.1	- Update branch office information
Mar. 10th, 2015	2.2	- Remove Encryption feature
Aug. 7th, 2015	2.3	- Add power parameter note

1.0 ATP Industrial Grade CFast Card Overview

1.1 ATP Product Image

Figure 1-1: ATP Product Image (reference only)

Table 1-1: Capacities

ATP P/N	CAPACITY
AF2GCSI-RABXP	2GB
AF4GCSI-RABXP	4GB
AF8GCSI-RABXP	8GB
AF16GCSI-RABXP	16GB
AF32GCSI-RABXP	32GB

Note: GB = 1,000,000,000 Byte

1.2 Introduction

With a form factor similar to CompactFlash card and a faster and more advanced SATA interface, ATP Industrial Grade CFast card is the ideal replacement of CompactFlash card. ATP Industrial Grade CFast card is fully compliant with CFA CFast specification version 1.1 with a SATA 3Gb/s interface. The CFast card contains a 24-pin connector consisting of a SATA compatible 7-pin signal connector and a 17-pin power and control connector. Compared to traditional CompactFlash card with ATA/IDE interface, ATP CFast card features high-speed data transfer capability of up to 80MB/s read speed, and a 65MB/s write speed.

By utilizing SLC NAND flash memory and Global Wear Leveling technology, the ATP Industrial Grade CFast cards have enhanced endurance levels and longer product life spans. The produce line implements ECC (Error Correction Code) and AutoRefresh technologies, which correct and monitor the error bit levels to ensure data integrity.

Incorporating the S.M.A.R.T. (Self-Monitoring, Analysis, and Reporting Technology) function, users are able to monitor various parameters of endurance and reliability. This information helps to predict storage failure with preventative action.

ATP PowerProtector technology guarantees reliable controller and lasting NAND flash operation with a back power circuit during a power outage. The standalone design of PowerProtector ensures a sufficient amount of backup power during any power abnormalities such as unstable voltages.

The new CFast specification, a combination of CF and ATA serial Transport (AST), is recommended as new boot and storage device in embedded and industrial markets. These markets include military/aerospace, automation, marine navigation, embedded system, telecommunication equipment/networking and medical equipment where mission-critical data requires the highest level of reliability, durability, and data integrity.

1.3 Main Features

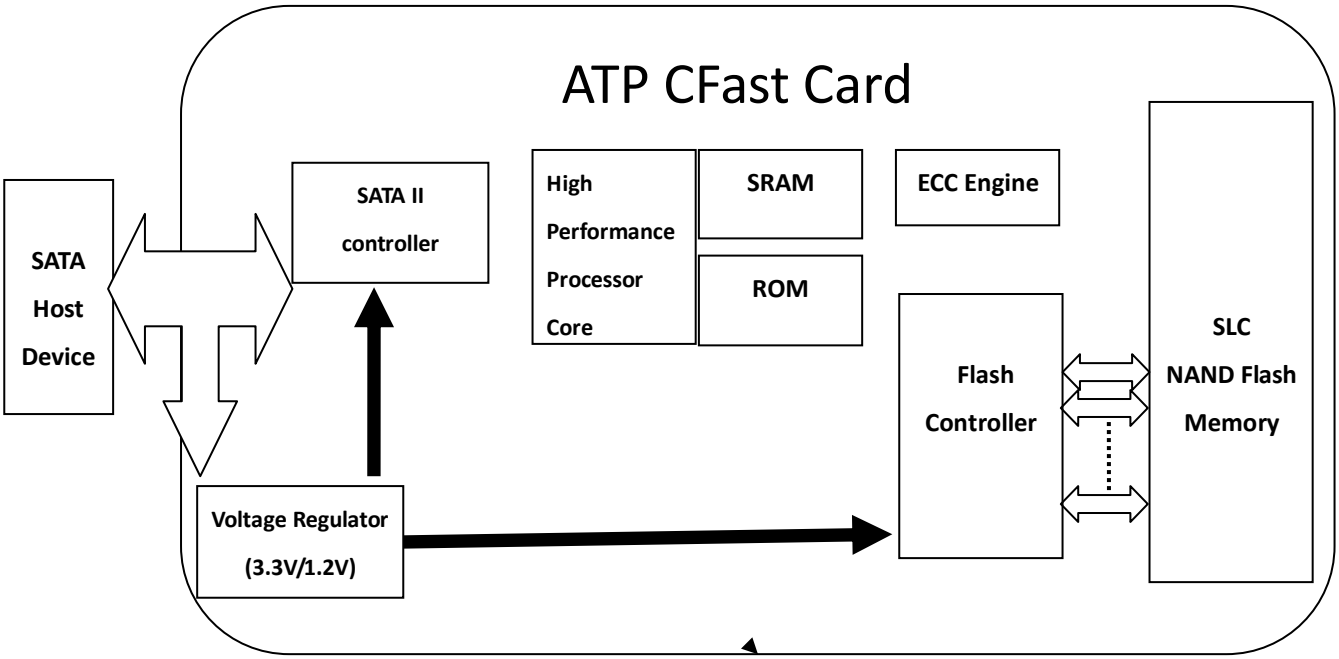
- Capacity: 2GB~32GB
- SLC (Single Level Cell) NAND flash memory
- Operating temperature: -40℃ to 85℃
- Maximum performance: Sequential read up to 80 MB/s, sequential write up to 65 MB/s
- Compliant with Serial ATA Revision 2.6 and CFast Specification 1.1
- Compatible with SATA 1.5Gbps and SATA 3Gbps interface rate
- 24-pin connector: 7-pin signal connector and 17-pin power and control connector
- Hardware BCH ECC, correct up to 24-bit ECC per 1024 bytes of data
- SMART function support by ATA CMD
- Enhanced endurance by Global wear-leveling
- AutoRefresh, automatic data protection in read operation
- PowerProtector Gen. 2, data protection under power-cycling
- CE, FCC certification

2.0 Product Specification

2.1 Block Diagram

ATP industrial grade CFast Card consists of below functional blocks. The advanced architecture is optimized to provide highest data reliability and transfer performance.

Figure 2-1:



2.2 Environment Specifications

Table 2-1

Type		Standard
Temperature	Operating	-40°C to 85°C
	Non-Operating	-40°C to 85°C
Humidity	Storage	40°C, 93% RH, noncondensing 85°C, 85% RH, noncondensing
Vibration (JESD22-B103)	Non-Operating	20G Peak, 20~2000Hz
Shock (JESD22-B110)	Non-Operating	1500G, 0.5ms duration, half sine wave
Altitude	Operating	80,000 feet Max.
	Non-Operating	80,000 feet Max.

2.3 IOPS Performance

Table 2-2

Type	Value
4K Random Read IOPS	Up to 3,300 IOPS

Note: IOPS: Input/Output operations per second tested by I/O meter on highest density.

2.4 Maximum Read/Write Performance

Table 2-3

Type		2GB	4GB	8GB	16GB	32GB
Crystal Disk Mark	Sequential Read (MB/s)	35	65	80	80	80
	Sequential Write(MB/s)	25	50	65	65	65

Note: Runs at SATA 3.0Gb/s host interface

2.5 Electrical Characteristics

Table 2-4

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Supply voltage	V_{CC}	3.15	3.3	3.45	V	

Note: Minimum timing of power off to power on is 300ms.

Table2-5

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Sustained write power	P_W	-	0.90	-	W	RMS value
Sustained read power	P_R	-	0.80	-	W	RMS value
Idle power	P_S	-	0.35	-	W	RMS value

2.6 Reliability

Table2-6

Type	Value
MTBF (@ 25°C) [1]	>2,000,000 hours
Data Retention (@ 40°C)	10 years (with 10% P/E cycle)

Notes: The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Telcordia SR-332, which based on reliability data of the individual components in the CFast. It assumes nominal voltage, with all other parameters within specified range.

2.7 Write/Erase Endurance[1]

Table 2-7

Type	Value
Number of Insertion	Min. 10,000 times
Endurance Technology	Enhanced global dynamic and static wear-leveling algorithm SLC Flash block in 2/4GB versions: 60,000 P/E cycles SLC Flash block in 8/16/32GB versions: 100,000 P/E cycles
SSD Endurance	2GB: 24TB random write 48TB sequential write 4GB: 48TB random write 96TB sequential write 8GB: 160TB random write 320TB sequential write 16GB: 320TB random write 640TB sequential write 32GB: 640TB random write 1,280TB sequential write

Note: Endurance for the CFast can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear leveling efficiency of the drive.

2.8 Certification and compliance

Table 2-9

Mark/Approval	Documentation	Certification
CE	The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French.	Yes
FC	FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts A and B (Sections 15.1 through 15.199) of FCC 47 CFR Part 15, usually called just FCC Part 15	Yes

3.0 CFast Pin Assignment

3.1 Pin Assignment

There are total of 7 pins in the signal segment and 17 pins in the power segment. The pin definitions are shown in Table 3-1

Table 3-1

Group	Pin No.[1]	Function	Description
Signal Segment	S1	GND	Ground
	S2	A+	Differential signal pair A
	S3	A-	
	S4	GND	Ground
	S5	B-	Differential signal pair B
	S6	B+	
	S7	GND	Ground
Key & Spacing			
Power Segment	P1	CDI	CMOS Input
	P2	GND	Device GND
	P3	TBD	TBD
	P4	TBD	TBD
	P5	TBD	TBD
	P6	TBD	TBD
	P7	GND	Device GND
	P8	LED1	LED output
	P9	LED2	LED output
	P10	IO1	Reserved input/output
	P11	IO2	Reserved input/output
	P12	IO3	Reserved input/output
	P13	PWR	Device power (3.3V)
	P14	PWR	Device power (3.3V)
	P15	GND	Device GND
	P16	GND	Device GND
	P17	CDO	Card detect out

3.2 Electrical Description

Table 3-2: Signal Description describes the I/O signals. Signals whose source is in the host are designated as inputs while signals that the CFast Card sources are outputs.

Table 3-2: Signal Description

Description of SATA Segment Pins

NAME	TYPE	DESCRIPTION
SGND	Signal Ground	These are intended to provide isolation for the high speed differential signals.
A+, A-, B+, B-	SATA Differential	The functionality and electrical characteristics of these pins are defined in the **SATA** reference

Description of PWR/CTL Segment Pins

NAME	TYPE	DESCRIPTION
CDI	CMOS Input	This signal is driven by the CFast host, and shall be sampled by the CFast device This pin shall be shorted on a CFast device to CDO. This signal and CDO provide a mechanism for a CFast host to detect that a CFast device has been fully inserted, and so that power can be applied safely. The host may drive, and the device may sample, this pin to provide signaling to enable CFast Power Management Sleep state.
CDO	CMOS Output	This pin shall be shorted on the CFast device to CDI. It is effectively driven by CDI.
LED1	LED Output	LED Output
LED2	LED Output	LED Output
IO1	CMOS Input/Output	Unassigned Input/Output pin
IO2	CMOS Input/Output	Unassigned Input/Output pin
IO3	CMOS Input/Output	Unassigned Input/Output pin

3.3 Electrical Specification

The tables in this section define all D.C. Characteristics for the CFast Card Series. Unless otherwise stated, conditions are:

Vcc = 3.3V ±5%

Ta = -40°C to 85°C

Table 3-3: Absolute Maximum Conditions

PARAMETER	SYMBOL	CONDITIONS
Input Power	Vcc	-0.3Vmin. to 3.6Vmax.
Voltage on any pin except Vcc with respect to GND.	V	-0.5Vmin. to Vcc + 0.5Vmax.

The card does not need to operate, or to meet any operating specifications outside its operating conditions. Application of absolute maximum conditions shall not damage the card.

3.3.1 Maximum input current

Table 3-31: Maximum Input Current

POWER LEVEL	Voltage Temperature During Test	Average Current Range (Active)	Average Current Range (Partial)	Average Current Range (Slumber)	Average Current Range (PHYSLP)
0	3.3V±1% at 23°C±1°C	0 – 500mA	0 – 500mA	0-250mA	0-20mA
1	3.3V±1% at 23°C±1°C	0 – 1200mA	0 – 1200mA	0-250mA	0-20mA

To comply with this specification, current requirements shall not exceed the maximum limit.

For CFast cards, two power levels are defined. Power Level 0 has a maximum average current of 500 mA, while Power Level 1 has an increased maximum current of 1200 mA for 3.3V. If the CFast card does not support the CFA Feature Set, the card shall stay within the power envelope of Power Level 1.

CFast cards shall operate within the specifications for Power Level 0 at power on and after reset. CFast cards shall also support ATA Identify Device and Set Features commands in Power Level 0. This requirement allows the host device to determine the CFast card's capabilities and which Power Levels are supported. The possibilities are:

Power Level 0,

Power Level 1,

Power Level 0 and Power Level 1.

The host shall use the Set Features command to set the desired power level to the card if it is compatible with it, or reject the CFast card.

An example of a CFast card using both Power Level 0 and Power Level 1 is a Flash memory card supporting both Power Levels. When set by the host to Power Level 0 (default) it shall have lower performance than when it is set to Power Level 1, but shall not exceed the Power Level 0 current consumption.

4.0 Command Set

4.1 ATA Command Set

ATP industrial grade CFast support the commands show in the following table

Table 4-1

Command	Code	Protocol
General Feature Set		
Execute Drive Diagnostic	90h	Device diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h or 21h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h or 31h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data

Command	Code	Protocol
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operation	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Return Status	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Save Attribute Values	B0h	Non-data
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out

4.2 Identity Device Data

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General Configuration
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete

Word Address	Default Value	Total Bytes	Data Field Type Information
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Obsolete
23-26	XXXXh	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	XXXXh	40	Model number in ASCII (Left justified) Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0F00h	2	Capabilities
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs) (Word57=LSW, Word58=MSW)
59	0100h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode (Word60=LSW, Word61=MSW)
62	0000h	2	Reserved
63	0007h	2	Multiword DMA transfer Supports MDMA Mode 0, 1, and 2
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word
66	0078h	2	Recommended Multiword DMA transfer cycle time
67	0078h	2	Minimum PIO transfer cycle time without flow control

Word Address	Default Value	Total Bytes	Data Field Type Information
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69~74	0000h	20	Reserved
75	0000h		Queue depth
76	0006h	2	Serial ATA capabilities Support Serial ATA Gen1 Support Serial ATA Gen2
	0206h		Support receipt of host-initiated interface power management requests
77	0000h	2	Reserved
78	0008h	2	SMART Read Data
79	0000h	2	Reserved
80	01FCh	2	Major version number (ATA8-ACS)
81	0000h	2	Minor version number
82	742Bh	2	Command sets supported 0
83	7500h	2	Command sets supported 1
84	4002h	2	Command sets supported 2
85~87	XXXXh	6	Command set/feature enabled
88	007Fh	2	Ultra DMA supported and selected
89	0003h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92	FFFEh	2	Master Password Revision Code
93~127	0000h	70	Reserved
128	0001h	2	Security status
129~159	0000h	62	Vendor unique bytes
160	0000h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported
163	0000h	2	CF Advanced True IDE Timing Mode Capability and Setting
164~216	0000h	106	Reserved
217	0100h	2	Non-rotating media(SSD)
218~255	0000h	76	Reserved

4.3 Smart Information

ATP industrial grade CFast card supports S.M.A.R.T. ATA feature set in IDE mode, AHCI mode, not support in RAID mode.

4.3.1 Smart Subcommand Sets

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands are listed below.

Table 4-3

Command	Command Code
SMART READ DATA	D0h
SMART READ ATTRIBUTE THRESHOLD	D1h
SMART ENABLE/DISABLE AUTOSAVE	D2h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMIDIATE	D4h
RESERVED	D5h
RESERVED	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh

Note: If the reserved size is below a threshold, status can be read from the Cylinder Register using the Return Status command (DAh)

4.3.2 SMART Read Data (Subcommand Doh)

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the “Read Data” command (D0h).

Table 4-4

Byte	F/V	Description
0~1	X	Revision code
2~361	X	Vendor Specific
362	V	Off-line data collection status
363	X	Self-test execution status byte

Byte	F/V	Description
364~365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor Specific
367	F	Off-line data collection capability
368~369	F	SMART capability
370	F	Error logging capability: 7-1 = Reserved 0 -1 = Device error logging supported
371	X	Vendor Specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375~385	R	Reserved
386~395	F	Firmware Version/Date Code
396~397	F	Reserved
398~399	F	Reserved
400~406	F	SMI2244LT
407~415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418~419	V	Number of spare block
420~423	V	Average erase count
424~510	X	Vendor Specific
511	V	Data structure checksum

Notes:

1. F=content (byte) is fixed and does not change
2. V=content (byte) is variable and maybe change depending on the state of the device or the command executed by the device
3. X= content (byte) is vendor specific and maybe fixed or variable
4. R=content (byte) is reserved and shall be zero

4.3.3 SMART Attribute

The following table defines the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

ID	Value (hex)	Raw Attribute Value						Attribute Name
1	01	MSB	00	00	00	00	00	Read error rate
5	05	LSB	MSB	00	00	00	00	Reallocated sectors count
9	09	LSB	MSB	00	00	00	00	Reserved
12	0C	LSB	MSB	00	00	00	00	Power cycle count
160	A0	LSB			MSB	00	00	Uncorrectable sector count when read/write
161	A1	LSB	MSB	00	00	00	00	Number of valid spare block
162	A2	LSB	MSB	00	00	00	00	Number of child pair
163	A3	LSB	MSB	00	00	00	00	Number of initial invalid block
164	A4	LSB			MSB	00	00	Total erase count
165	A5	LSB			MSB	00	00	Maximum erase count
166	A6	LSB			MSB	00	00	Minimum erase count
167	A7	LSB			MSB	00	00	Average erase count
192	C0	LSB			MSB	00	00	Power-off retract count
194	C2	MSB	00	00	00	00	00	Controlled temperature (Fixed at 27^{o}C)
195	C3	LSB			MSB	00	00	Hardware ECC Recovered
196	C4	LSB			MSB	00	00	Reallocation Event count
198	C6	LSB			MSB	00	00	Reserved
199	C7	LSB	MSB	00	00	00	00	UltraDMA CRC error count

ID	Value (hex)	Raw Attribute Value						ID
241	F1	LSB			MSB	00	00	Total LBAs written (each write unit=32MB)
242	F2	LSB			MSB	00	00	Total LBAs read (each write unit=32MB)

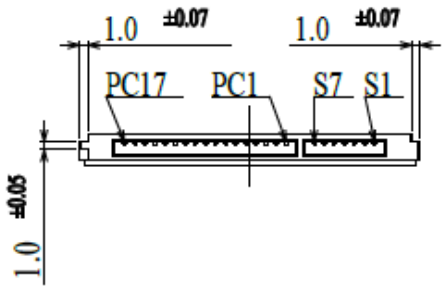
5.0 Mechanical Information

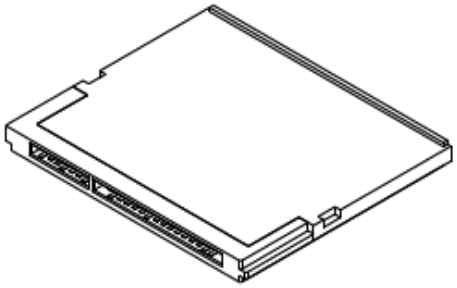
5.1 Physical Dimension Specifications

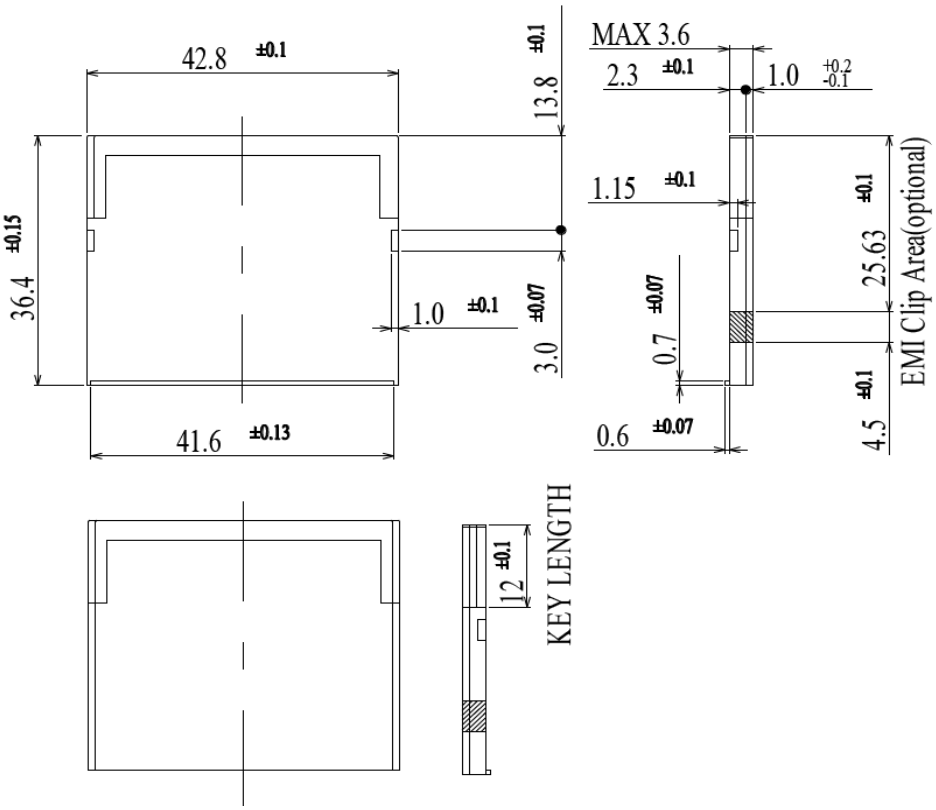
Table 5-1

Type		Value
CFast (Type I)	Length	36.40 mm +/- 0.15mm
	Width	42.80 mm +/- 0.10 mm
	Thickness	max. 3.6 mm

5.2 Mechanical Form Factor (Units in mm)







ATP TAIWAN(HQ)
TEL: +886-2-2659-6368
FAX: +886-2-2659-4982
sales-apac@atpinc.com

ATP USA
TEL: +1-408-732-5000
FAX: +1-408-732-5055
sales@atpinc.com

ATP JAPAN
TEL: +81-03-6206-8097
FAX: +81-03-6206-8098
sales-japan@atpinc.com

ATP EUROPE
TEL: +49-89-374-9999-0
FAX: +49-89-374-9999-29
sales-europe@atpinc.com

ATP CHINA
TEL: +86-21-5080-2220
FAX: +86-21-5080-2219
sales@cn.atpinc.com

www.atpinc.com